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**SYSTEM AND METHOD FOR ADDRESSING MEMORY AND
TRANSFERRING DATA**

Abstract

10 A system and method for addressing memory and transferring data, which in
some embodiments include one or more processor translation look-aside buffers (TLBs)
and optionally one or more I/O TLBs, and/or a block transfer engine (BTE) that
optionally includes a serial cabinet-to-cabinet communications path (MLINK). In some
embodiments, the processor TLBs are located within one or more common memory
sections, each memory section being connected to a plurality of processors, wherein
each processor TLB is associated with one of the processors. The BTE performs
15 efficient memory-to-memory data transfers without further processor intervention. The
MLINK extends the BTE functionality beyond a single cabinet.

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